multi-layered interconnect structure, previously described as solder balls or columns 20, are placed in contact with the solder paste on the contact pads of the circuitized substrate. The solder paste and second plurality of solder connections are reflowed and cooled forming an electrical connection between the multi-layered interconnect structure and the circuitized substrate. The sequence of assembly of the semiconductor chip to the multi-layered interconnect structure, followed by assembly of the multi-layered interconnect structure to the circuitized substrate, can easily be modified so that the multi-layered interconnect structure without the semiconductor chip can be assembled to the circuitized substrate followed by assembly of the semiconductor chip tot he multi-layered interconnect structure-circuitized substrate assembly.

In the Claims

Claims 82 and 88 are amended herein, as marked up in Appendix A. Currently pending claims 80-97 for consideration by the Examiner are as follows:

80. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first